Protection of Tombstone Problems for Small Chip Devices

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Abstract:

Small chip components (Such as #0402 or #0603 Chip Device) may have “tombstone” problems during the solder paste reflow process. Tombstoning is a phenomenon where the chip component is raised and detached from the printed circuit board at one end while remaining bonded to the circuit board at the opposite end. In this case the chip component takes a vertical orientation.

The tombstone effect is caused by a difference in the length of time at which the solder paste is melted at opposite ends of the component during heating in a reflow furnace. When the melting of solder paste adhering to the first electrode at one end of the chip component occurs earlier than that solder adhering to the second electrode located at the opposite end, the earlier melted solder paste acts to pull down the first electrode by the surface tension force of the molten solder, thus creating tombstone problems on PCB sub-assembly process.

In this case the tombstone problem may be dramatically reduced by adjusting the area between the liquidus and solidus temperatures. Use of a two (2) peak melting point alloy (as shown by a Differential Scanning Calorimeter (DSC)) has proven very effective for tombstone problems by keeping a good equality balance with power of moment at both sides of the chip device electrode.

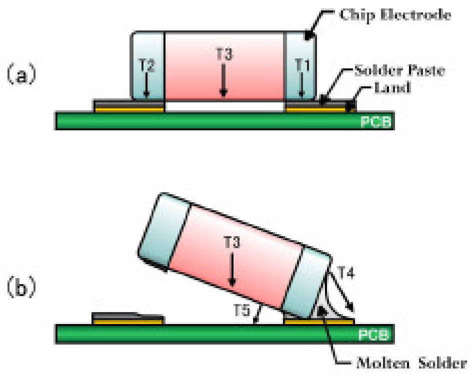
Therefore, We found that the two (2) peak melting point alloy, while keeping the majority of other types of single peak alloy characteristics, had the following results when considering the various data between two (2) peak alloy’s solder paste and tombstone problem:

- -Two (2) peak temperature alloy solder paste dramatically reduced the tombstone effect.
- -Two (2) peak temperature solder alloy data indicates improvement for creep and thermal cycle testing results compared to eutectic solder.

Introduction:

Electronics manufacturing companies are developing many different kinds of small electric packages and high technology products such as the Cellular Phone, Video Camera and Notebook PC. Therefore, manufacturers require small chip components such as chip capacitors(chip condenser) or resistance with high performance for sub-assembly.

The small chip components (Such as #0402, #0603 Chip Device) may have tombstone problems during the solder paste reflow process.



$$T4>T2+T3+T5$$

T1,T2 : Moment of tack force power with solder paste.
T3 : Moment of self weight with chip device.
T4 : Moment of melting solder sueface tension at chip device Electro area.
T5 : Moment of melting solder surface tension at under the chip device.

Figure 1 Several different kind of Moments for effort to chip device at reflow process.
(a) Solder paste condition just before melting at reflow process.
(b) Condition of melting solder at only one side Electro when temperature is different at both side of Electro with chip device.

Fig-1 illustrates chip component conditions during several different moments of the reflow process.

We may see a moment difference between melting solder side and non-melting solder side when both sides of the chip device electrode area have a different temperature during the reflow process. Tombstone problems may occur when the force of moment T4 (surface tension at one side of the chip device electrode area) is larger than the sum of moment T3 (self weight), moment T5 (surface tension under the chip device) and moment T2 (tack force power at the opposite side of chip device electrode area).

While his phenomena is finished in less than one (1) second, Sn63 Pb37 eutectic alloy's solder paste has a tendency of allowing this tombstone problem when compared to other compositions of solders. Because the Sn63 Pb37 eutectic solder does not have the semi-molten area between the liquidus and solidus temperature and immediately melts the melting solder's surface tension cannot maintain an equal balance for power of moment at both sides of the chip device electrode area.

We may consider many different methods for improvement of this phenomena such as; exchanging soldering pad designs on PCB, maintaining the accuracy of the chip device mounting machine, adjusting the temperature profile for reflow and modifying flux vehicles and/or the solder alloy composition of solder paste.

However, in the case of high density types of PCB sub-assembly or installing a large thermal device near small chip devices such as the #0402, we have a very high risk of seeing tombstone problems because of the temperature differences between both sides of the chip device.

In this case, we may reduce the tombstone effect by making adjustments to the solder melting temperature area between the liquidus and solidus line and by slowly melting the solder. This allows the surface tension to the both sides of the chip devices electrode area to slowly increase without suddenly melting the solder paste at one side.

Actual method of tombstone protection with the above theory is:

-Development of a twin peak temperature solder alloy by Differential Scanning Calorimeter (DSC).

-Peak temperatures range within 10 degrees C. (To minimize risk of solder crack)

-Maintain the same temperature profile for new material as standard Sn63 Pb37 eutectic solder.

This report considered different alloy compositions, the development of a new high performance solder paste and analyzed for comparison data between several different kinds of alloys (paste) and the new Senju developed solder paste (Sn62 Ag0.4 Sb0.2 Pb balance).

We also analyzed some alloy characteristics for Sn63 Pb37 eutectic alloy and Sn62 Ag0.4 Sb0.2 Pb balance alloy such as creep and thermal cycle tests.

DSC (Differential Scanning Calorimeter)

We analyzed adding elements and volume to the Sn63 Pb37 eutectic alloy in order to develop a twin peak alloy solder paste with tombstone protection.

By adding only small amounts of other elements, the twin peak alloy's condition becomes a ternary eutectic alloy. We determined that the silver (Ag) element was the best choice after many tests.

Fig-2 – 8
Fig-2: Sn63 Pb37, Fig-3: Sn62Ag0.1Sb0.2 Pb Balance,
Fig-4: Sn62 Ag0.3 Sb0.2 Pb Balance
Fig-5: Sn62 Ag0.4 Sb0.2 Pb Balance, Fig-6: Sn62 Ag0.5 Sb0.2 Pb Balance,
Fig-7: Sn62 Ag0.7 Sb0.2 Pb Balance, Fig-8: Sn62.5 Ag1.35 Pb Balance,

Fig-2 is DSC data for Sn63 Pb37 eutectic alloy. (reference)

Fig-3 --- Fig-7 are DSC data for Sn Pb based eutectic, adding 0.2% Sb and various other elements containing 0.1 ---0.7% of Ag material.

This DSC data expresses that 0.2% of Sb does not effect the solder melting temperature, however, the Ag material does have an effect on the solder melting temperature. This means that when 0.1wt% Ag is added the (Fig-3) Ag_3 Sn + (Pb) + (Sn) ternary alloy begins to melt at 177.5^{o}C first, then the (Sn) + (Pb) eutectic solder portion begins to melt at 182.0 ^{o}C next. This tendency shows the same results up to a 0.7wt% Ag content. The Ag_3Sn + (Pb) + (Sn) ternary alloy melting temperature will increase above 177.5^{o}C when Ag volume is increased.

Considering the tombstone problem by DSC data, we may expect good results with the alloy of Ag0.3 --- 0.5wt% showing a clearly visible twin peak temperature condition.

Fig-8 is eutectic temperature peak of Ag_3Sn + (Pb) + (Sn) alloy as indicated by the DSC data of the standard eutectic alloy.

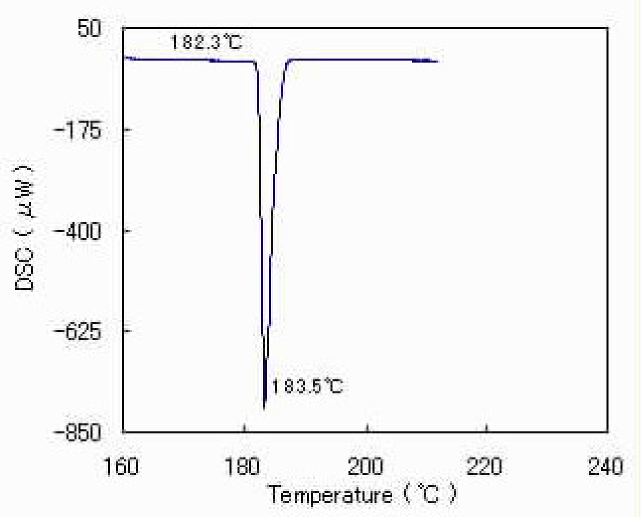


Figure 2 DSC of Sn63 PB37 Alloy

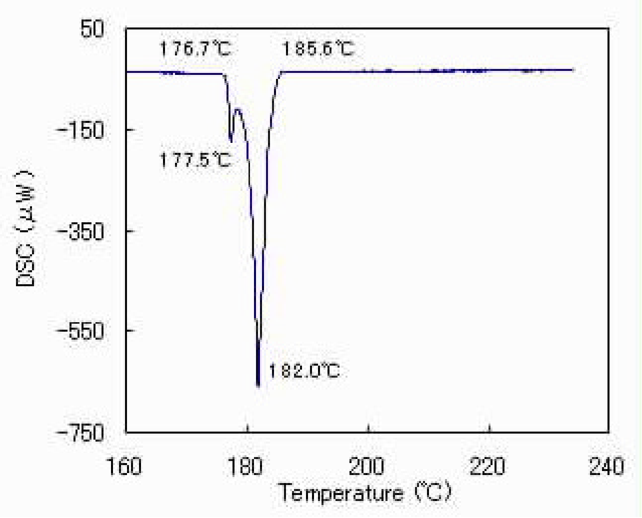


Figure 3 DSC of Sn62 Ag0.1 Sb0.2 Pb Balance

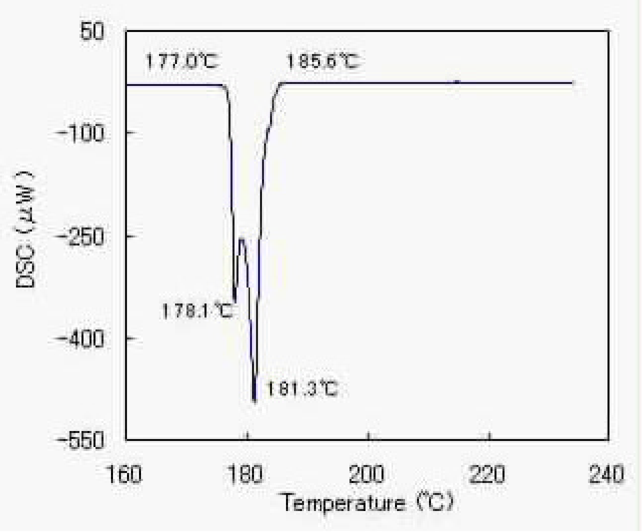


Figure 4 DSC of Sn62 Ag0.3 Sb0.2 Pb Balance

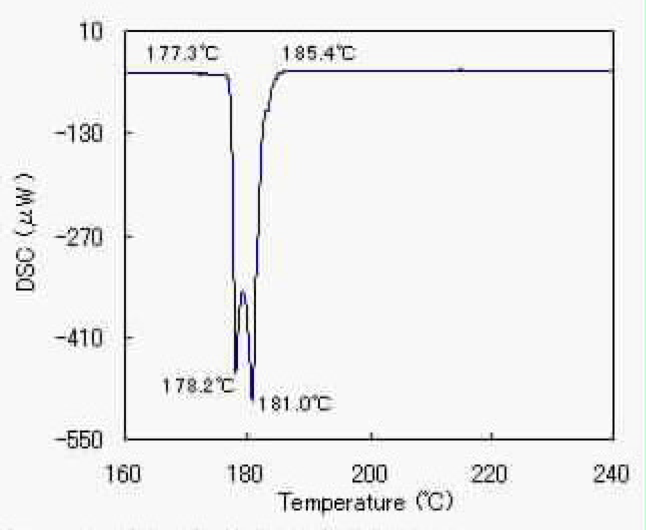


Figure 5 DSC of Sn62 Ag0.4 Sb0.2 Pb Balance

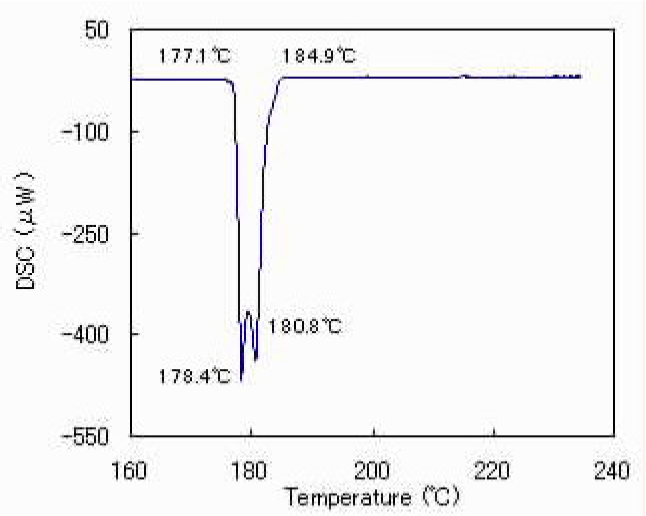


Figure 6 DSC of Sn62 Ag0.5 Sb0.2 Pb Balance

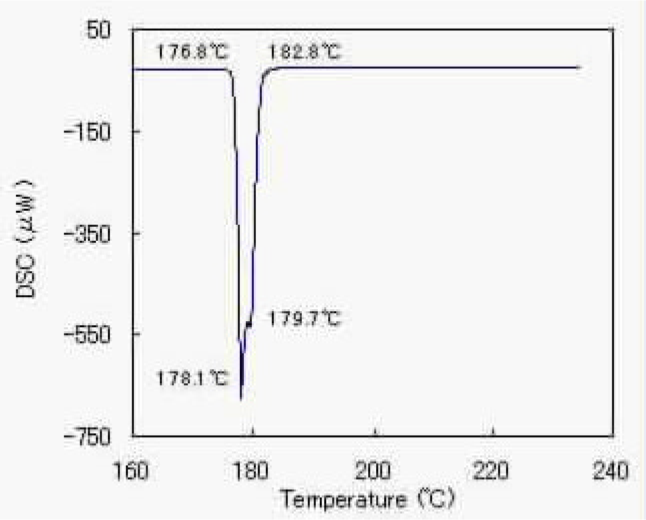


Figure 7 DSC of Sn62 Ag0.7 Sb0.2 Pb Balance

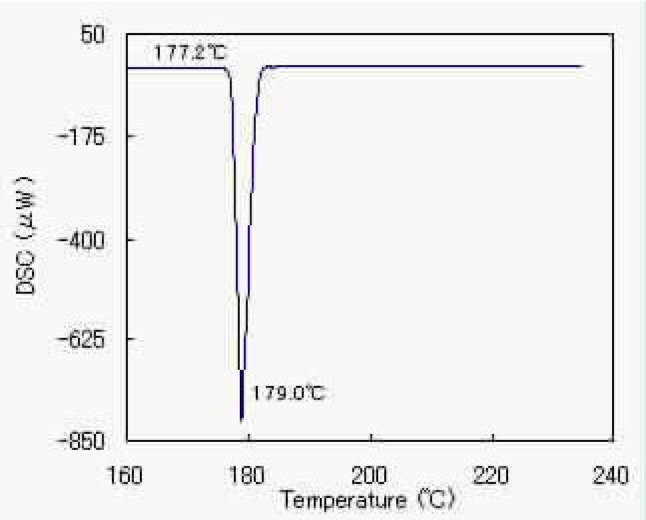


Figure 8 DSC of Sn62.5 Ag1.35 Pb Balance

Tombstone problem test with #0402 chip device (Capacitor)

We obtained the Sn62 Ag0.4 Sb0.2 Pb balance alloy which clearly indicates a twin peak temperature profile by DSC testing. We believe this solder to be very effective with tombstone problems.

Table-1 shows characteristics for 6 different kind of tested solder pastes with Sn62 Ag0.4 Sb0.2 Pb balance alloy and Sn63 Pb37 eutectic solder alloy.

Table 1 Characteristics of evaluated Solder Paste

Item	1	2	3	4	5	6	Remark
Composition (wt %)	Sn 63 Pb 37	Sn 62 Ag 0.1 Sb 0.2 Pb 37.7	Sn 62 Ag 0.3 Sb 0.2 Pb 37.5	Sn 62 Ag 0.4 Sb 0.2 Pb 37.4	Sn 62 Ag 0.5 Sb 0.2 Pb 37.3	Sn 62 Ag 0.7 Sb 0.2 Pb 37.1	ASTM B-32
Particle size (μm)	25～45	25～45	25～45	25～45	25～45	25～45	J-STD-005 IPC-TM-650 2.2.14
Flux (Senju RMA)	221CM5	221CM5	221CM5	221CM5	221CM5	221CM5	
Flux Content (wt %)	10.10	10.08	9.99	9.97	10.02	10.07	J-STD-005 IPC-TM-650 2.2.20
Halide Content (Cl, wt %)	0.049	0.042	0.042	0.043	0.044	0.046	J-STD-004 IPC-TM-650 2.3.35
Viscosity (Malcom,P)	1900	1910	1810	1730	1800	1870	J-STD-005 IPC-TM-650 2.4.34
Thixo-Index	0.71	0.70	0.68	0.67	0.68	0.69	J-STD-005 IPC-TM-650 2.4.34
Slump test (mm)	0.4 0.4	0.3 0.4	0.3 0.4	0.4 0.4	0.4 0.4	0.4 0.5	JIS Z 3284 Annex 8

6 different kind of solder pastes were applied on each different FR-4 PCB by a screen printing method as described below, #0402 chip devices were then mounted on these solder pastes and run through reflow by standard reflow temperature profile.

Measurements were taken for tombstone problems with both conditions and the outbreak ratio was calculated.

However, we could not easily obtain a large number of tombstone problems with the standard sub-assembly conditions. Therefore, We used the following bad test conditions intentionally in order to increase the occurrence of tombstone problems.

Reflow oven: Nitrogen convection reflow oven (Oxygen level 100ppm)
Reflow process: Chip device mounting side inverted to run upside down inside reflow oven.
Solder Paste: RMA No-Clean type with type-3 powder distribution
And 6 different solder paste (Table-1)
Stencil tickles: 0.12mm (5 mil)
PCB: FR-4 100 x 110 x 1.2mm
Pad: 0.6mm circle
Pad space: 0.6mm
Chip device: #0402 chip capacitor by Murata Electric
Number of Chip device: 320 pieces / PCB x 15
Chip mounting machine: SMT-2500 (Full vision placement system) by Suzuki Co.,Ltd

Fig-9 is a photograph of sub-assembly of Sn63 Pb37 eutectic and Sn62 Ag0.4 Sb0.2 Pb balance alloy's solder paste after reflow.

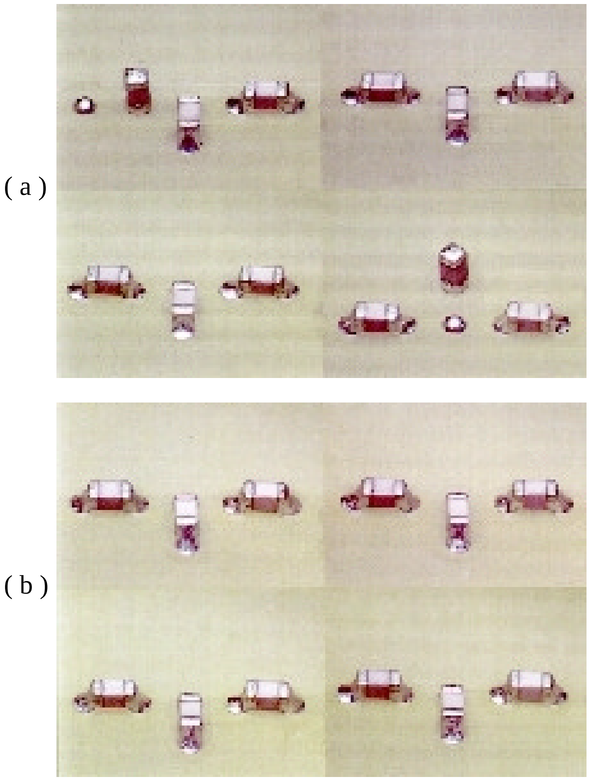


Figure 9 Photograph of sub-assembly alloy's solder paste after reflow
(a) Sn63 Pb37
(b) Sn62 Ag0.4 Sb0.2 Pb Balance

Table-2 and Figure-10 shows test results for #0402 chip device with tombstone problem. The results declare that the Sn62 Ag0.4 Sb0.2 Pb balance alloy produced fewer than 10% of the tombstone problems compared to the Sn63 Pb37 eutectic solder.

Another twin peak alloy's pastes such as Ag0.1 and Ag0.7 also improve the tombstone problem relative to the Sn63 Pb37 eutectic alloy's paste. But those pastes have a higher number of tombstone problems than Sn62 Ag0.4 Sb0.2 Pb balance alloy's paste. (These test results are in good proportion to the DSC data.)

This test as performed by Senju used an intentionally bad test condition for creating tombstone problems such as an inverted PCB running inside reflow oven.

Current actual electronics products are using high density sub-assembly applications for small PCB areas which may easily obtain tombstone problems and we cannot avoid the presence of high density PCB sub-assembly applications. Therefore, this test condition very closely duplicates a real sub-assembly application and we can expect the Sn62 Ag0.4 Sb0.2 Pb balance alloy's solder paste to assist in the elimination of tombstone problems with high density products.

Table 2 Results of Tombstone Test

Sample No. (320 Chips/PCB)	Solder Alloy					
	Sn63 Pb37 Alloy	Sn62 Ag0.1 Sb0.2 pb Alloy	Sn62 Ag0.3 Sb0.2 pb Alloy	Sn62 Ag0.4 Sb0.2 pb Alloy	Sn62 Ag0.5 Sb0.2 pb Alloy	Sn62 Ag0.7 Sb0.2 pb Alloy
1	1	0	0	0	0	0
2	0	1	0	0	0	0
3	0	1	0	0	0	0
4	5	0	0	1	0	3
5	0	0	0	0	0	0
6	5	5	0	0	0	0
7	8	1	1	0	0	1
8	0	0	0	0	0	0
9	3	0	0	0	0	2
10	1	4	0	0	1	0
11	8	0	0	0	0	0
12	0	3	0	1	0	1
13	0	0	4	0	1	0
14	2	0	0	0	0	0
15	0	5	0	0	0	9
Total of Tombstones	33	20	5	2	2	16
Total of Chips	4800	4800	4800	4800	4800	4800
% of Tombstones	0.69	0.42	0.10	0.04	0.04	0.33

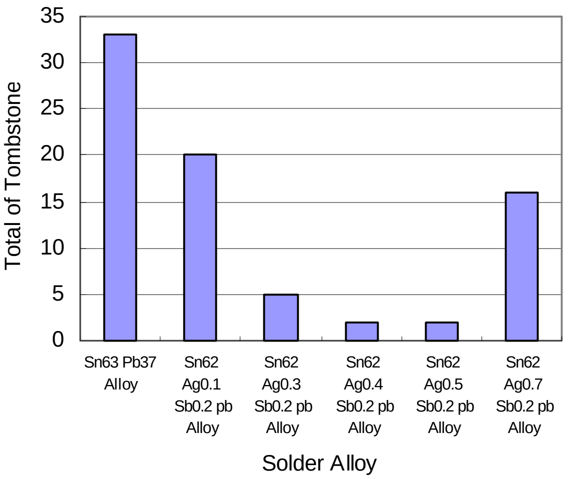


Figure 10 Results of Tombstone Test

Reliability Test of Sn62 Ag0.4 Sb0.2 Pb balance alloy

(1) Creep Test at soldering joint

Made test piece like a Fig-11 with copper wire by soldering. Copper wire was then soldered to the test PCB in order to apply weight. Creep time was then measured inside the high temperature chamber.

Test piece Condition:

Test PCB FR-4

Through hole round pad diameter 3mm

Hole diameter 1mm

Cu (Copper) lead diameter 0.7mm

Solder Volume 20mg

Test condition: High temperature chamber 100 °C

Fig-12 is test results for soldering joint creep test.

Sn62 Ag0.4 Sb0.2 Pb balance alloy is about 2 times more strong for creep test result than Sn63 Pb37 eutectic solder alloy.

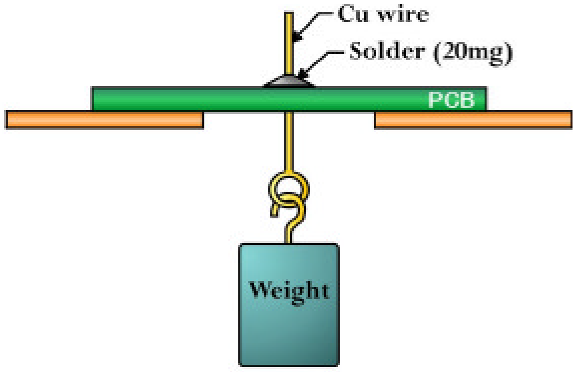


Figure 11 Schematic of Creep Test

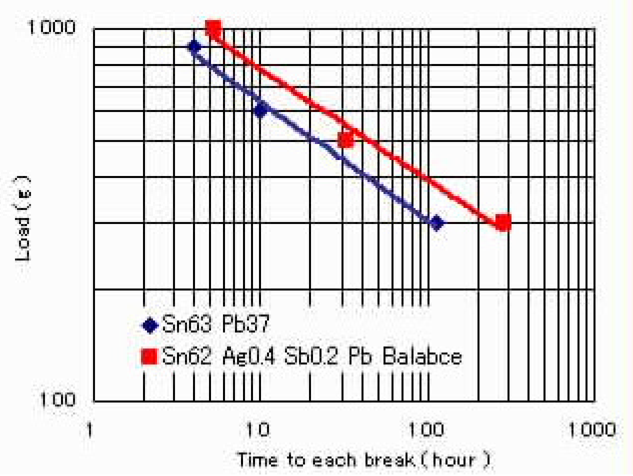


Figure 12 : Results of Creep Test at 100°C

(2) Thermal cycle test

To conduct thermal cycle testing, Senju made a test piece with a nylon connector soldered onto an FR-3 PCB with Sn62 Ag0.4 Sb0.2 Pb balance alloy. We also made the same test piece with Sn63 pb37 eutectic solder for reference.

Note: Choice of nylon connector and FR-3 (paper phenol) was made to easily obtain solder cracking condition compared to FR-4. The FR-3 material is a more difficult test platform because FR-3's thermal expansion ratio is about 10 times larger than FR-4.

FR-3 's CTE = 196 x 10^{-6} / °C with thick direction.

Nylon's CTE = 80 – 100 x 10^{-6} / °C

Counting of solder crack problem with thermal cycle condition.

PCB:	FR-3 single layer Size 45 x 75 x 1.6mm Through hole round diameter 2mm Hole diameter 1mm
Connector:	8 pins nylon material
Test Piece:	Nylon connector soldering on FR-3 PCB.
Test condition:	Test piece installed to thermal cycle chamber with -40 °C with 30min to +80 °C with 30min.

Fig-13 shows various test results data for the thermal cycle and crack outbreak ratio. This data indicates that Sn62 Ag0.4 Sb0.2 Pb balance alloy is about 2 times stronger material than the Sn63 Pb37 eutectic solder when both alloys obtained a 10% of crack outbreak ratio. (Sn62 Ag0.4 Sb0.2 Pb balance alloy met 10% ratio at 560 cycles, Sn63 Pb37 at 330 cycles.)

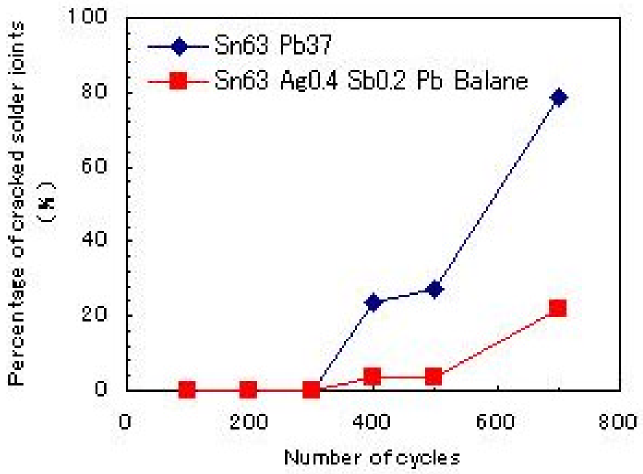


Figure 13 Number of thermal cycles vs.
Percentage of cracked solder joints.

Conclusions

We obtained the following test results regarding the relationship between solder alloy composition and tombstone problems.

- Manufactured a new solder alloy composition with a twin peak melting temperature (DSC) having a very close reflow temperature profile to standard eutectic alloy.
- This new alloy's solder paste assists in the elimination of tombstone problems with #0402 small chip device. Also, We obtained data which indicates a relationship between twin peak temperature and tombstone problem ratio. This means that this solder alloy is effective with high density PCB sub-assemblies for protecting tombstone issues.
- This new material alloy composition consists of the base Sn63 Pb37 eutectic alloy and the addition of 0.4% of silver (Ag) material and 0.2% antimony (Sb) to increase creep and thermal cycle characteristics as well.

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